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<u>L23</u>	15 and 111	1	<u>L23</u>
<u>L22</u>	15 and 110	1	<u>L22</u>
<u>L21</u>	15 and 19	3	<u>L21</u>
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<u>L19</u>	15 and 17	26	<u>L19</u>
<u>L18</u>	15 and 16	26	<u>L18</u>
<u>L17</u>	14 and 111	3	<u>L17</u>
<u>L16</u>	14 and 110	6	<u>L16</u>
<u>L15</u>	14 and 19	5	<u>L15</u>
<u>L14</u>	14 and 18	0	<u>L14</u>
<u>L13</u>	14 and 17	37	<u>L13</u>

<u>L12</u>	14 and 16	37	<u>L12</u>
<u>L11</u>	(713/320)[CCLS]	1272	<u>L11</u>
<u>L10</u>	(713/310-340)![CCLS]	3657	<u>L10</u>
<u>L9</u>	(711/169,173)![CCLS]	1557	<u>L9</u>
<u>L8</u>	(712/213,209,207,219,227)[CCLS]	1829	<u>L8</u>
<u>L7</u>	(712/2-300)[CCLS]	12348	<u>L7</u>
<u>L6</u>	(712/2-300)![CCLS]	12348	<u>L6</u>
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<u>L5</u>	L3 and pipelin\$7 near12 (fetch\$5 or prefetch\$5)	134	<u>L5</u>
<u>L4</u>	L3 and pipelin\$7	299	<u>L4</u>
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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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



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Solomon, B.; Mendelson, A.; Ronen, R.; Orenstien, D.; Almog, Y.;  
[Very Large Scale Integration \(VLSI\) Systems. IEEE Transactions on](#)  
Volume 11, Issue 5, Oct. 2003 Page(s):801 - 811  
Digital Object Identifier 10.1109/TVLSI.2003.814327  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1496 KB) IEEE JNL  
[Rights and Permissions](#)
- ☐ 2. **Combined circuit and architectural level variable supply-voltage scaling for low power**  
Hai Li; Chen-Yong Cher; Roy, K.; Vijaykumar, T.N.;  
[Very Large Scale Integration \(VLSI\) Systems. IEEE Transactions on](#)  
Volume 13, Issue 5, May 2005 Page(s):564 - 576  
Digital Object Identifier 10.1109/TVLSI.2005.844295  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(688 KB) IEEE JNL  
[Rights and Permissions](#)
- ☐ 3. **VSV: L2-miss-driven variable supply-voltage scaling for low power**  
Hai Li; Chen-Yong Cher; Vijaykumar, T.N.; Roy, K.;  
[Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposium](#)  
2003 Page(s):19 - 28  
Digital Object Identifier 10.1109/MICRO.2003.1253180  
[AbstractPlus](#) | Full Text: [PDF](#)(332 KB) IEEE CNF  
[Rights and Permissions](#)
- ☐ 4. **Proceedings 30th Annual International Symposium on Computer Architecture**  
[Computer Architecture, 2003. Proceedings. 30th Annual International Symposium on](#)  
9-11 June 2003  
Digital Object Identifier 10.1109/ISCA.2003.1206983  
[AbstractPlus](#) | Full Text: [PDF](#)(245 KB) IEEE CNF  
[Rights and Permissions](#)
- ☐ 5. **Saving energy with just in time instruction delivery**  
Karkhanis, T.; Smith, J.E.; Bose, P.;  
[Low Power Electronics and Design, 2002. ISLPED '02. Proceedings of the 2002 International Symp](#)  
2002 Page(s):178 - 183  
[AbstractPlus](#) | Full Text: [PDF](#)(605 KB) IEEE CNF  
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-  **6. Energy-efficient register access**  
 Tseng, J.H.; Asanovic, K.;  
[Integrated Circuits and Systems Design, 2000. Proceedings. 13th Symposium on](#)  
 18-24 Sept. 2000 Page(s):377 - 382  
 Digital Object Identifier 10.1109/SBCCI.2000.876058  
[AbstractPlus](#) | Full Text: [PDF](#)(468 KB) [IEEE CNF](#)  
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-  **7. Power efficiency through application-specific instruction memory transformations**  
 Petrov, P.; Orailoglu, A.;  
[Design, Automation and Test in Europe Conference and Exhibition, 2003](#)  
 2003 Page(s):30 - 35  
 Digital Object Identifier 10.1109/DATE.2003.1253583  
[AbstractPlus](#) | Full Text: [PDF](#)(279 KB) [IEEE CNF](#)  
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-  **8. Stage-skip pipeline: a low power processor architecture using a decoded instruction buffer**  
 Hiraki, M.; Bajwa, R.S.; Kojima, H.; Gorny, D.J.; Nitta, K.; Shri, A.;  
[Low Power Electronics and Design, 1996. International Symposium on](#)  
 12-14 Aug. 1996 Page(s):353 - 358  
 Digital Object Identifier 10.1109/LPE.1996.547538  
[AbstractPlus](#) | Full Text: [PDF](#)(560 KB) [IEEE CNF](#)  
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-  **9. Reducing power consumption of dedicated processors through instruction set encoding**  
 Benini, L.; De Micheli, G.; Macii, A.; Macii, E.; Poncino, M.;  
[VLSI, 1998. Proceedings of the 8th Great Lakes Symposium on](#)  
 19-21 Feb. 1998 Page(s):8 - 12  
 Digital Object Identifier 10.1109/GLSV.1998.665191  
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-  **10. An adiabatic framework for a low energy /spl mu/-architecture and compiler**  
 Ramarao, P.; Tyagi, A.;  
[Interaction Between Compilers and Computer Architectures, 2003. INTERACT-7 2003. Proceeding on](#)  
 8 Feb. 2003 Page(s):65 - 72  
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-  **11. Enhancing loop buffering of media and telecommunications applications using low-overhead**  
 Sias, J.W.; Hunter, H.C.; Hwu, W.-M.W.;  
[Microarchitecture, 2001. MICRO-34. Proceedings. 34th ACM/IEEE International Symposium on](#)  
 1-5 Dec. 2001 Page(s):262 - 273  
 Digital Object Identifier 10.1109/MICRO.2001.991124  
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